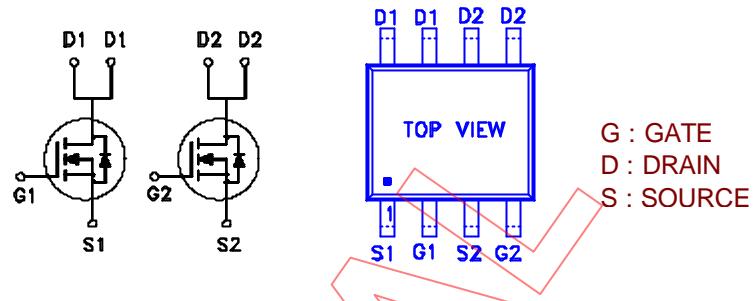


NIKO-SEM
**Dual N-Channel Enhancement Mode
Field Effect Transistor**
P2002IVG
SOP-8
Lead-Free
PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
20	20m	7A

**ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ Unless Otherwise Noted)**

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 12	V
Continuous Drain Current	$T_C = 25^\circ\text{C}$	I_D	7	A
	$T_C = 70^\circ\text{C}$		6	
Pulsed Drain Current ¹		I_{DM}	38	
Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	2	W
	$T_C = 70^\circ\text{C}$		1.3	
Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	$^\circ\text{C}$
Lead Temperature (1/16" from case for 10 sec.)		T_L	275	

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Ambient	$R_{\theta JA}$		62.5	$^\circ\text{C} / \text{W}$

¹Pulse width limited by maximum junction temperature.²Duty cycle $\leq 1\%$ **ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$, Unless Otherwise Noted)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu\text{A}$	20			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	0.5	0.8	1.2	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 12V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 16V, V_{GS} = 0V$			1	μA
		$V_{DS} = 16V, V_{GS} = 0V, T_J = 55^\circ\text{C}$			10	
On-State Drain Current ¹	$I_{D(\text{ON})}$	$V_{DS} = 5V, V_{GS} = 4.5V$	15			A

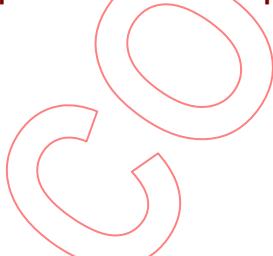
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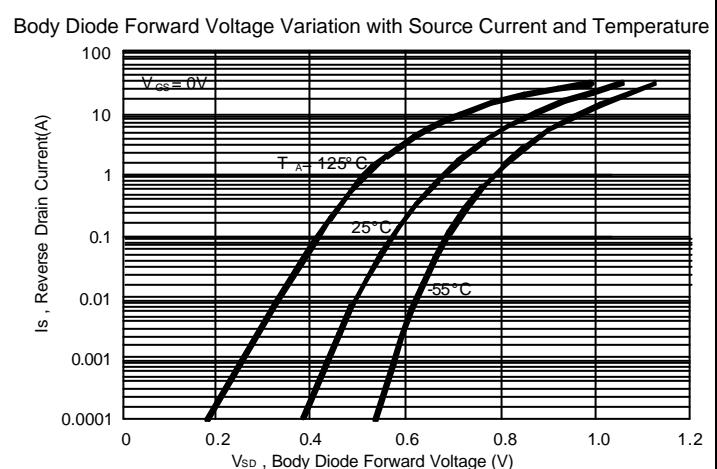
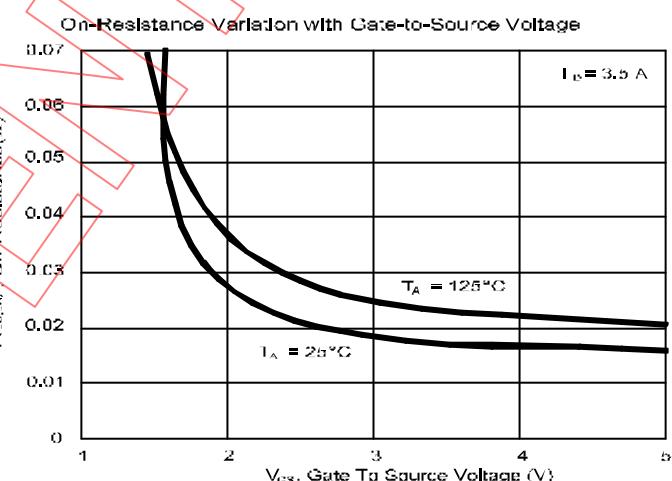
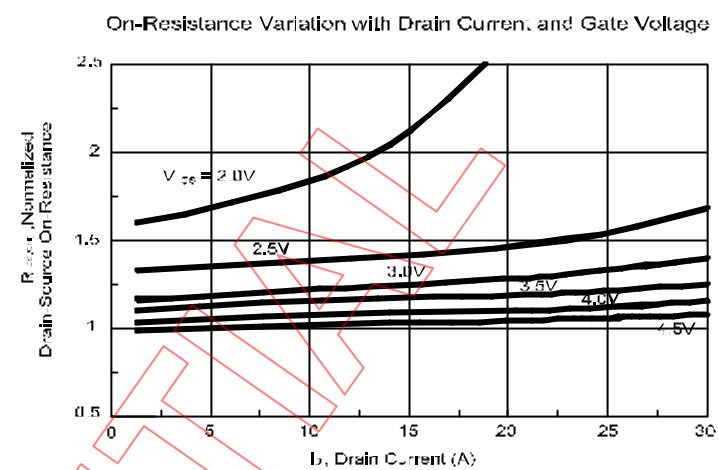
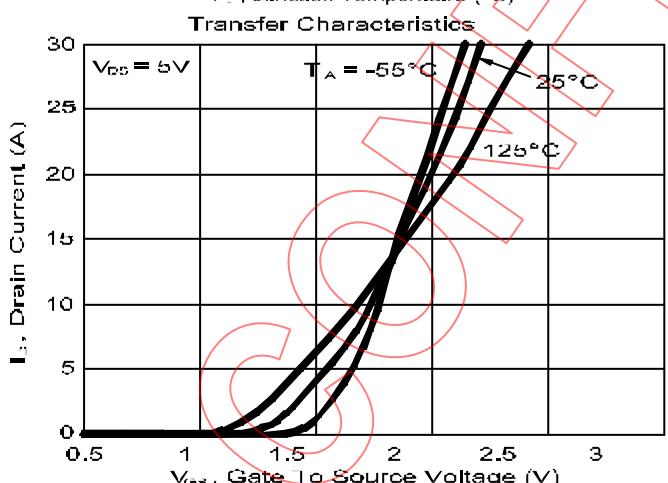
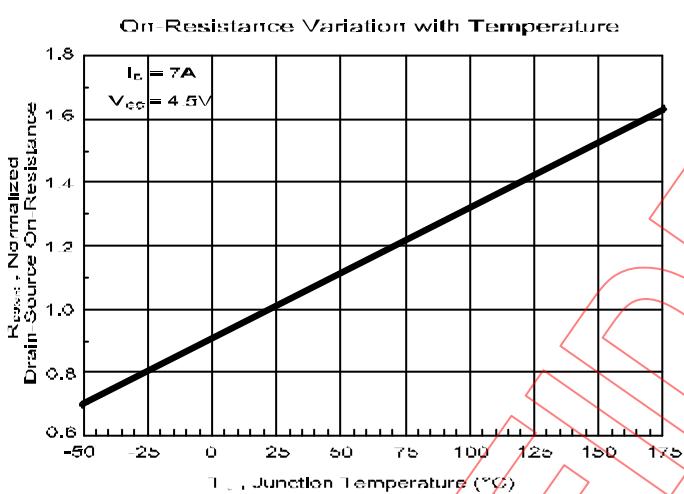
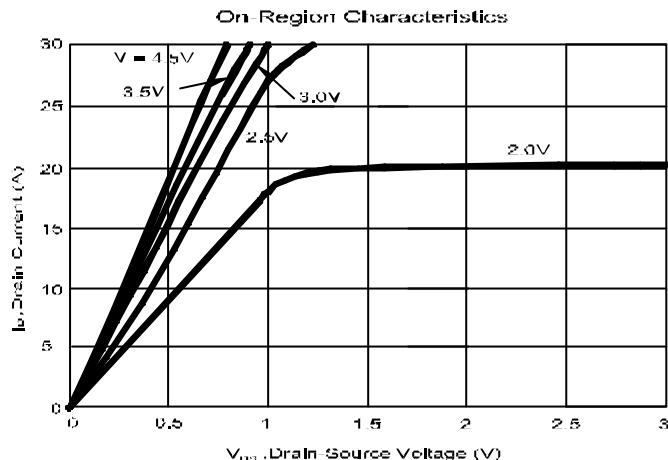
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 2.5V, I_D = 6A$	21	35	m
		$V_{GS} = 4.5V, I_D = 7A$	15	21	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 7A$	37		s
DYNAMIC					
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 10V, f = 1MHz$	1082		pF
Output Capacitance	C_{oss}		277		
Reverse Transfer Capacitance	C_{rss}		130		
Total Gate Charge ²	Q_g		12	19	
Gate-Source Charge ²	Q_{gs}	$V_{DS} = 0.5V_{(BR)DSS}, V_{GS} = 4.5V, I_D = 7A$	2		nC
Gate-Drain Charge ²	Q_{gd}		3		
Turn-On Delay Time ²	$t_{d(on)}$		8	16	
Rise Time ²	t_r	$V_{DS} = 10V$ $I_D \approx 1A, V_{GS} = 4.5V, R_{GEN} = 6$	8	16	nS
Turn-Off Delay Time ²	$t_{d(off)}$		24	38	
Fall Time ²	t_f		8	16	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_C = 25^\circ C$)					
Continuous Current	I_S	$I_F = 1A, V_{GS} = 0V$		1.3	A
Pulsed Current ³	I_{SM}			2.5	
Forward Voltage ¹	V_{SD}	$I_F = 5A, dI_F/dt = 100A/\mu S$		1.2	V
Reverse Recovery Time	t_{rr}		15.5		
Reverse Recovery Charge	Q_{rr}		7.9		

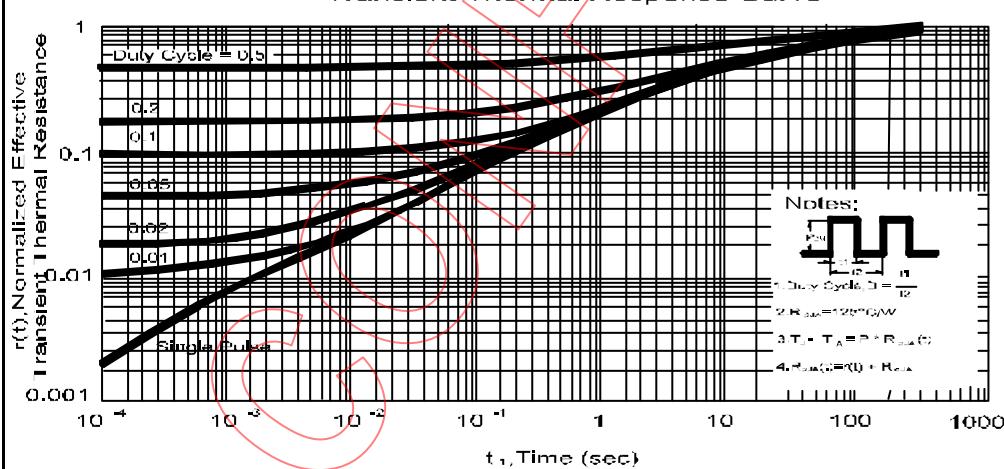
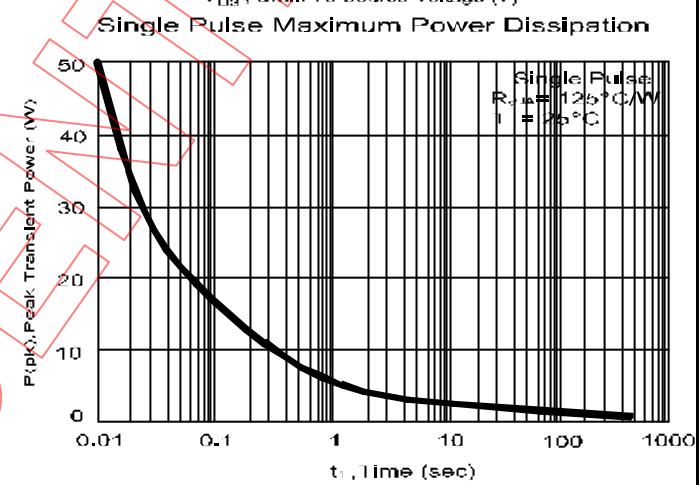
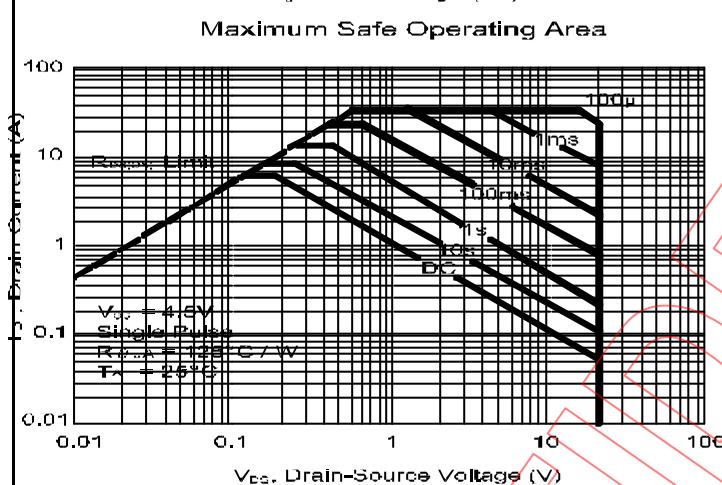
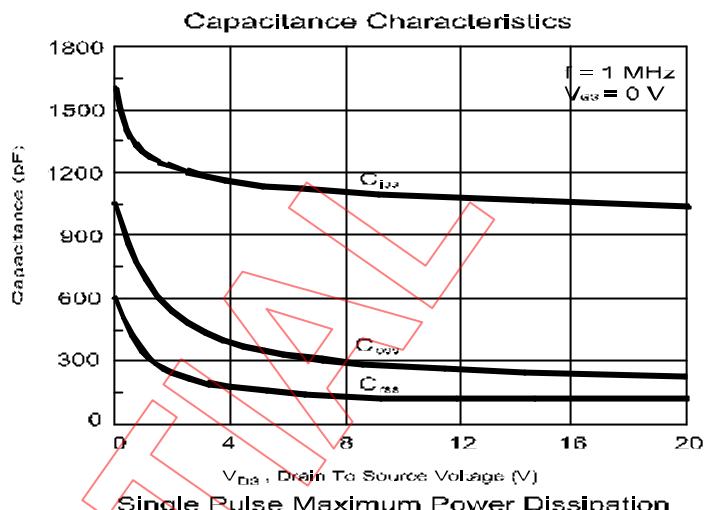
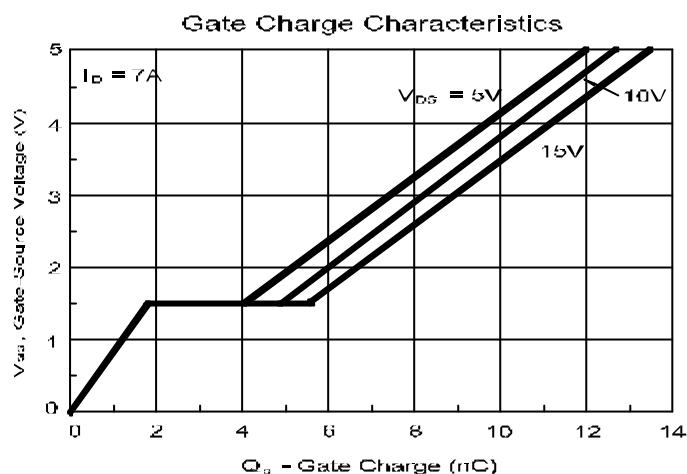
¹Pulse test : Pulse Width ± 300 msec, Duty Cycle $\pm 2\%$ ²Independent of operating temperature.³Pulse width limited by maximum junction temperature.

REMARK: THE PRODUCT MARKED WITH "P2002IVG", DATE CODE or LOT #

Orders for parts with Lead-Free plating can be placed using the PXXXXXXG parts name.



NIKO-SEM
**Dual N-Channel Enhancement Mode
Field Effect Transistor**
P2002IVG
SOP-8
Lead-Free
TYPICAL PERFORMANCE CHARACTERISTICS


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Notes:
 1. Duty Cycle, $D = \frac{t}{T}$
 2. $R_{JA} = 125^{\circ}\text{C}/\text{W}$
 3. $T_f = T_a + P \cdot R_{JA} \cdot D$
 4. $R_{JA}(D=0) = R_{JA}$

SOIC-8(D) MECHANICAL DATA

Dimension	mm			Dimension	mm		
	Min.	Typ.	Max.		Min.	Typ.	Max.
A	4.8	4.9	5.0	H	0.5	0.715	0.83
B	3.8	3.9	4.0	I	0.18	0.254	0.25
C	5.8	6.0	6.2	J		0.22	
D	0.38	0.445	0.51	K	0°	4°	8°
E		1.27		L			
F	1.35	1.55	1.75	M			
G	0.1	0.175	0.25	N			

